SPECIFICATION AMENDMENTS

Replace the paragraph beginning at page 2, line 12 with:

With reference to Figs. ~~2 and 3~~2A to 3B, details of the surge voltage occurring at the cable connection ends of the motor 2 are described. Figs. ~~2 and 3~~2A to 3B are drawings that depict line-to-line voltage waveforms at both ends of the connection cable 3 shown in Fig. 1.

Replace the paragraph beginning at page 2, line 16 with:

Fig. ~~2 (1)~~2A depicts a case where an inverter-end line-to-line voltage Vuv_inv is varied stepwise as Vdc→0→Vdc. At this time, when a pulse width in voltage change coincides with half of a resonant cycle, as shown in Fig. ~~2 (2)~~2B, a motor-end line-to-line voltage Vuv_motor becomes three times as high as the direct-current bus voltage Vdc at maximum.

Replace the paragraph beginning at page 2, line 23 with:

Also, Fig. ~~3 (1)~~3A depicts a case where the inverter-end line-to-line voltage Vuv_inv is varied stepwise as 0→Vdc→-Vdc→0. At this time, as shown in Fig. ~~3 (2)~~3B, the motor-end line-to-line voltage Vuv_motor becomes four times as high as the direct-current bus voltage Vdc at maximum.

Replace the paragraph beginning at page 3, line 2 with:

From the description with reference to Figs. ~~2 and 3~~2A to 3B, it is known that if the pulse width in voltage change is sufficiently large, after resonance occurring due to a stepwise voltage change is attenuated, the next stepwise voltage change is applied, and therefore a surge voltage exceeding twice the direct-current bus voltage Vdc does not occur.

Replace the paragraph beginning at page 4, line 20 with:

It is an object of the present invention to solve at least the above problems in the conventional technology. An apparatus ~~according to one aspect of the present invention, which is~~ for controlling a power converter ~~in which an output voltage is controlled by a~~

~~pulse-width-modulation control,~~ according to one aspect of the present invention includes a voltage-vector control unit that determines, based on a voltage instruction value for the power converter, a voltage vector output from the power converter in one control cycle of the pulse-width-modulation control and ~~a~~ time ~~to output~~ of outputting of the voltage vector; a voltage-vector adjusting unit that adjusts the time ~~to output~~ of outputting of the voltage vector in such a manner that ~~a~~ the time ~~to output~~ of outputting of a zero-voltage vector ~~is ensured at least for~~ is longer than a ~~constant~~ fixed time or zero; and a firing-pulse generating unit that generates a signal for turning on and off a semiconductor switching element included in the power converter, based on the time ~~to output~~ of outputting of the voltage vector as adjusted by the voltage-vector adjusting unit.

Delete the paragraph beginning at page 5, line 8:

~~According to this aspect of the present invention, the zero-voltage-vector output time is ensured to be always equal to or larger than a predetermined value. Therefore, a resonant phenomenon associated with switching of the semiconductor elements can be attenuated while the zero-voltage vectors are being output, thereby effectively suppressing a surge voltage exceeding twice the direct-current bus voltage.~~

Delete the paragraph beginning at page 5, line 15:

~~An apparatus according to another aspect of the present invention, which is for controlling a power converter in which an output voltage is controlled by a pulse-width-modulation control, includes a voltage-vector control unit that determines, based on a voltage instruction value for the power converter, a voltage vector output from the power converter in one control cycle of the pulse-width-modulation control and a time to output the voltage vector; a voltage-vector adjusting unit that adjusts the time to output the voltage vector in such a manner that when a time to output a zero-voltage vector is longer than a predetermined time, the time to output the zero-voltage vector is ensured at least for a constant time, and when the time to output the zero-voltage vector is shorter than the predetermined time, the time to output the zero-voltage vector is set to zero; and a firing-pulse generating unit that generates a signal for turning on and off a semiconductor switching element included in the power converter based on the time to output the voltage vector adjusted by the voltage-vector adjusting unit.~~

Delete the paragraph beginning at page 6, line 7:

~~According to this aspect of the present invention, either one of providing a zero-voltage-vector output time equal to or larger than a predetermined value and making the zero-voltage-vector output time zero is selected based on the concept of rounding off. With this, a surge voltage exceeding twice the direct-current bus voltage can be suppressed.~~

Delete the paragraph beginning at page 6, line 13:

~~An apparatus according to still another aspect of the present invention, which is for controlling a power converter in which an output voltage is controlled by a pulse-width-modulation control, includes a voltage-vector control unit that determines, based on a voltage instruction value for the power converter, a voltage vector output from the power converter in more than one control cycle of the pulse-width-modulation control and a time to output the voltage vector; a voltage-vector adjusting unit that adjusts the time to output the voltage vector in more than one control cycle of the pulse-width-modulation control in such a manner that, when a total of a time to output a zero-voltage vector in more than one control cycle is shorter than a predetermined time, the time the output the zero-voltage vector between two adjacent cycles is set to zero and an amount of the time to output the zero-voltage vector between the two adjacent cycles is distributed to the time to output the zero-voltage vector in control cycles next to the two adjacent cycles; and a firing-pulse-generating unit that generates a signal for turning on and off a semiconductor switching element included in the power converter based on the time to output the voltage vector adjusted by the voltage-vector adjusting unit.~~

Delete the paragraph beginning at page 7, line 7:

~~According to this aspect of the present invention, when a plurality of control cycles equal to or more than two control cycles of the pulse-width-modulation control are taken as a unit, a zero-voltage vector located between two adjacent cycles is eliminated, thereby doubling the remaining output times of the zero-voltage vectors. Consequently, for one control cycle, the total of the output times of the voltage vectors other than the zero-voltage vectors does not have to be changed until the total of the output times of the zero-voltage vectors becomes less than a predetermined value, thereby reducing error. According to this method, a zero-voltage-vector output time equal to or larger than the predetermined value is~~

~~provided, or the zero-voltage-vector output time is made zero. Therefore, as with the aspect of the present invention mentioned above, a surge voltage exceeding twice the direct-current bus voltage can be suppressed.~~

Delete the paragraph beginning at page 7, line 21:

~~An apparatus according to still another aspect of the present invention, which is for controlling a power converter in which an output voltage is controlled by a pulse-width-modulation control, includes a voltage-vector control unit that determines, based on a voltage instruction value for the power converter, a voltage vector output from the power converter in more than one control cycle of the pulse-width-modulation control and a time to output the voltage vector; a voltage-vector adjusting unit that adjusts the time to output the voltage vector in more than one control cycle of the pulse-width-modulation control in such a manner that, when a total of a time to output a zero-voltage vector in more than one control cycle is shorter than a predetermined time, times to output same voltage vectors in more than one control cycle are added; and a firing-pulse generating unit that generates a signal for turning on and off a semiconductor switching element included in the power converter based on the time to output the voltage vector adjusted by the voltage-vector adjusting unit.~~

Delete the paragraph beginning at page 8, line 13:

~~According to this aspect of the present invention, when a plurality of control cycles equal to or more than two control cycles of the pulse-width-modulation control are taken as a unit, output times of same voltage vectors in the control cycles equal to or more than two control cycles are collected as one, thereby doubling the output times of the voltage vectors including the zero-voltage vectors. Consequently, for one control cycle, the total of the output times of the voltage vectors other than the zero-voltage vectors does not have to be changed until the total of the output times of the zero-voltage vectors becomes less than a predetermined value, thereby reducing error. According to this method, the zero-voltage-vector output time is ensured to be always equal to or larger than a predetermined value. Therefore, as with the aspects of the present invention mentioned above, a surge voltage exceeding twice the direct-current bus voltage can be suppressed.~~

Delete the paragraph beginning at page 9, line 3:

~~An apparatus according to still another aspect of the present invention, which is for controlling a power converter in which an output voltage is controlled by a pulse-width-modulation control, includes a voltage-vector control unit that determines, based on a voltage instruction value for the power converter, a voltage vector output from the power converter in one control cycle of the pulse-width-modulation control and a time to output the voltage vector; a voltage-vector adjusting unit that adjusts the time to output the voltage vector in such a manner that, when a time to output a zero-voltage vector is shorter than a predetermined value, upon receiving a voltage vector used for an adjustment in a previous control cycle, depending on whether a vector lastly output in the previous cycle is a zero-voltage vector, one of times to output a zero-voltage vector at a current cycle is set to zero and an amount of the one of the times is distributed to other of the times; a delay unit that delays the voltage vector output from the voltage-vector adjusting unit by the one control cycle, and outputs the voltage vector to the voltage-vector adjusting unit; and a firing-pulse generating unit that generates a signal for turning on and off a semiconductor switching element included in the power converter based on the time to output the voltage vector adjusted by the voltage-vector adjusting unit.~~

Delete the paragraph beginning at page 9, line 24:

~~According to this aspect of the present invention, the voltage vectors are adjusted so that the zero-voltage vectors located at the first and last of the pulse-width control cycle are combined as one, thereby doubling the output times of the zero-voltage vectors. Consequently, the total of the output times of the voltage vectors other than the zero-voltage vectors does not have to be changed until the total of the output times of the zero-voltage vectors becomes less than a predetermined value, thereby reducing error. According to this method, a zero-voltage-vector output time equal to or larger than the predetermined value is provided, or the zero-voltage-vector output time is made zero. Therefore, as with the aspects of the present invention mentioned above, a surge voltage exceeding twice the direct-current bus voltage can be suppressed.~~

Delete the paragraph beginning at page 10, line 12:

~~An apparatus according to still another aspect of the present invention, which is for controlling a power converter in which an output voltage is controlled by a pulse-width-modulation control, includes a voltage-vector control unit that determines, based on a voltage instruction value for the power converter, a voltage vector output from the power converter in one control cycle of the pulse-width-modulation control and a time to output the voltage vector, a voltage-vector adjusting unit that adjusts the time to output the voltage vector in such a manner that, upon receiving a voltage vector used for an adjustment in a previous control cycle and a time to output the voltage vector, when a total of a first time to output a zero-voltage vector lastly adjusted in the previous cycle and a second time to output a zero-voltage vector firstly in a current cycle is shorter than a predetermined time, the second time is adjusted to be a time obtained by subtracting the first time from the predetermined time; a delay unit that delays the voltage vector output from the voltage-vector adjusting unit by the one control cycle, and outputs the voltage vector to the voltage-vector adjusting unit; and a firing pulse generating unit that generates a signal for turning on and off a semiconductor switching element included in the power converter based on the time to output the voltage vector adjusted by the voltage-vector adjusting unit.~~

Delete the paragraph beginning at page 11, line 8:

~~According to this aspect of the present invention, with the use of the adjusted output time of the zero-voltage vector last output in the previous pulse-width-modulation control cycle, an output time of a zero-voltage vector to be output in the current cycle is determined. Therefore, the output time of the zero-voltage vector can be ensured to be equal to or larger than a predetermined value even when the zero-voltage vector extends over the pulse-width-modulation control cycles. Therefore, as with the aspects of the present invention mentioned above, a surge voltage exceeding twice the direct-current bus voltage can be suppressed.~~

Delete the paragraph beginning at page 11, line 18:

~~An apparatus according to still another aspect of the present invention, which is for controlling a power converter in which an output voltage is controlled by a pulse-width-modulation control, includes a voltage-vector control unit that determines, based on a voltage instruction value for the power converter, a voltage-vector output from the power converter in~~

~~one control cycle of the pulse-width modulation control and a time to output the voltage vector; a voltage-vector adjusting unit that adjusts the time to output the voltage vector, including a function of calculating an error accompanied by an adjustment of the time to output the voltage vector, in such a manner that, regarding a time to output a voltage vector obtained by correcting the voltage vector in a current cycle with the error calculated in a previous cycle, when a time to output a zero-voltage vector is longer than a predetermined time, the time to output the zero-voltage vector is ensured at least for a constant time, and when the time to output the zero-voltage vector is shorter than the predetermined time, the time to output the zero-voltage vector is set to zero; a delay unit that delays the voltage vector output from the voltage-vector adjusting unit by the one control cycle, and outputs the voltage vector to the voltage-vector adjusting unit; and a firing-pulse generating unit that generates a signal for turning on and off a semiconductor switching element included in the power converter based on the time to output the voltage vector adjusted by the voltage-vector adjusting unit.~~

Delete the paragraph beginning at page 12, line 16:

~~According to this aspect of the present invention, as with the aspects of the present invention mentioned above, a surge voltage exceeding twice the direct-current bus voltage can be suppressed. Furthermore, with the use of the adjustment error in the previous pulse-width-modulation control cycle, the output times of the voltage vectors to be output in the current cycle are corrected, thereby eliminating influences of the previous adjustment. Therefore, the end point of the present locus of the magnetic flux vector can agree with a desired point, and fluctuations in the locus of the magnetic flux vector associated with suppression of a surge voltage can be minimized.~~

Delete the paragraph beginning at page 13, line 1:

~~According to the one aspect of the present invention, the voltage-vector adjusting unit adjusts the time to output the voltage vector in such a manner that the time to output the zero-voltage vector is ensured at least for the constant time without changing a relative ratio of output times of voltage vectors other than the zero-voltage vector.~~

Delete the paragraph beginning at page 13, line 7:

~~According to this aspect of the present invention, with the contrivance in the adjustment of the voltage vectors, fluctuations in the locus of the magnetic flux vector associated with suppression of a surge voltage can be minimized.~~

Delete the paragraph beginning at page 13, line 11:

~~According to the another aspect of the present invention, the voltage vector adjusting unit adjusts the time to output the voltage vector in such a manner that, when the time to output the zero voltage vector is set to zero, times to output voltage vectors other than the zero voltage vector are set to longer than the constant time or set to zero, too.~~

Delete the paragraph beginning at page 13, line 17:

~~According to this aspect of the present invention, when the output time of the zero voltage vectors are adjusted to be zero, a surge voltage may occur depending on the output time of non zero voltage vectors other than the zero voltage vectors. However, such a surge voltage can be restricted according to this aspect. Therefore, a surge voltage exceeding twice the direct current bus voltage can be reliably suppressed.~~

Delete the paragraph beginning at page 13, line 24

~~According to the another aspect of the present invention, upon setting the time to output the zero voltage vector set to zero, when the voltage vector lastly output in the previous cycle is different from the voltage vector firstly output in the current cycle, the voltage vector adjusting unit changes the voltage vector firstly output in the current cycle to the voltage vector lastly output in the previous cycle.~~

Delete the paragraph beginning at page 14, line 5:

~~According to this aspect of the present invention, when the output time of the zero voltage vectors are adjusted to be zero, a surge voltage may occur depending on the output time of non zero voltage vectors other than the zero voltage vectors. However, such a surge voltage can be restricted according to this aspect. Therefore, a surge voltage exceeding twice~~

~~the direct-current bus voltage can be reliably suppressed.~~

Delete the paragraph beginning at page 14, line 12:

~~Furthermore, according to each aspect of the present invention, the adjustment of the voltage-vector output times is performed on the output times of the voltage vectors, which are parameters that are generated based on three-phase voltage instructions and are common to three phases. Therefore, with one adjustment, an effect of suppressing a surge voltage can be obtained over all phases.~~

Insert paragraph at page 14, line 18:

Other objects, features, and advantages of the present invention will become apparent from the following detailed description of the invention when read in conjunction with the accompanying drawings.

Replace the Brief Description of the Drawings section with:

Fig. 1 is a drawing for explaining a connection cable between an inverter, which is a power converter driven by PWM control, and a motor;

~~Fig. 2 is a~~ Figs. 2A and 2B are (first) ~~drawing~~ drawings that ~~depicts~~ illustrate line-to-line voltage waveforms between both ends of the connection cable shown in Fig. 1;

~~Fig. 3 is a~~ Figs. 3A and 3B are (second) ~~drawing~~ drawings that ~~depicts~~ illustrate line-to-line voltage waveforms between both the ends of the connection cable shown in Fig. 1;

Fig. 4 is a block diagram depicting the structure of a power-converter control apparatus according to a first embodiment of the present invention;

Fig. 5 is a circuit diagram depicting a basic structure of a three-phase voltage inverter for use in the embodiment as the power converter driven by PWM control;

Fig. 6 is a drawing for explaining a relation between turned-on IGBT elements and voltage vectors in eight control states of the inverter shown in Fig. 5;

Fig. 7 is a drawing for explaining voltage vectors;

Fig. 8 is a drawing for explaining a relation between phases and voltage vectors;

Fig. 9 is a flowchart for explaining the operation of a voltage-vector adjusting unit shown in Fig. 4;

~~Fig. 10 is a diagram~~ Figs. 10A and 10B are diagrams for explaining loci of magnetic

flux vectors when the voltage vectors are adjusted;

Fig. 11 is a time chart for explaining the operation of a firing-pulse generating unit shown in Fig. 4;

~~Fig. 12 is a drawing~~ Figs. 12A to 12D are drawings for explaining a relation between the progression of the voltage vectors and line-to-line voltages;

Fig. 13 is a drawing that depicts line-to-line voltage patterns extracted in view of a pulse polarity, an output time of zero-voltage vectors, and an output time of voltage vectors other than the zero-voltage vectors;

~~Fig. 14 is a drawing~~ Figs. 14A to 14H are drawings for explaining surge voltages occurring due to the line-to-line voltages shown in Fig. 13;

Fig. 15 is a flowchart for explaining the operation of a voltage-vector adjusting unit included in a controlling device for the power controller according to a second embodiment of the present invention;

Fig. 16 is a block diagram depicting the structure of a power-converter control apparatus according to a third embodiment of the present invention;

Fig. 17 is a flowchart showing a voltage-vector adjusting unit shown in Fig. 16;

Fig. 18 is a flowchart for explaining the operation of a voltage-vector adjusting unit included in a power-converter control apparatus according to a fourth embodiment of the present invention;

Fig. 19 is a block diagram showing a power-converter control apparatus according to a fifth embodiment of the present invention;

Fig. 20 is a flowchart for explaining the operation of a voltage-vector adjusting unit shown in FIG. 19;

Fig. 21 is a flowchart for explaining the operation of a voltage-vector adjusting unit included in a power-converter control apparatus according to a sixth embodiment of the present invention;

Fig. 22 is a block diagram depicting the structure of a power-converter control apparatus according to a seventh embodiment of the present invention;

Fig. 23 is a flowchart for explaining the operation of a voltage-vector adjusting unit shown in Fig. 22;

~~Fig. 24 is a drawing~~ Figs. 24A to 24C are drawings for explaining an error-calculating operation to be performed by the voltage-vector adjusting unit shown in Fig. 22;

Fig. 25 is a flowchart for explaining the operation of a voltage-vector adjusting unit included in a power-converter control apparatus according to an eighth embodiment of the present invention; and

Fig. 26 is a flowchart for explaining the operation of a voltage-vector adjusting unit included in a power-converter control apparatus according to a ninth embodiment of the present invention.

Delete paragraph beginning at page 17, line 2:

~~First Embodiment~~

Replace the paragraph beginning at page 21, line 11 with:

Next, with reference to Figs. 9 and ~~10~~ 10A to 10C, the operation of the voltage-vector adjusting unit 12 is described. Fig. 9 is a flowchart for explaining the operation of the voltage-vector adjusting unit shown in Fig. 4. ~~Fig. 10 is a diagram~~ Figs. 10A-10C are diagrams for explaining loci of magnetic flux vectors when the voltage vectors are adjusted.

Replace the paragraph beginning at page 22, line 2 with:

As a result, if the total output time t0+t7 of the zero-voltage vectors is longer than the minimum zero-voltage-vector output time Tz ~~(step ST11: Yes)~~(step ST11: No), the read output times t1, t2, t0, and t7 are directly taken as t1', t2', t0', and t7' (step ST12).

Replace the paragraph beginning at page 22, line 23 with:

As described above, when the voltage vectors are adjusted, a locus of a magnetic flux vector obtained through integration of the voltages can be drawn as shown in ~~Fig. 10~~ Figs. 10A to 10C. In Fig. ~~10 (1)~~10A, a locus A of a magnetic flux vector for one PWM control cycle before adjustment of the voltage vectors is depicted. In Fig. ~~10 (2)~~10B, a locus A' of the magnetic flux vector after adjustment of the voltage vectors is depicted. As a result of ensuring the minimum zero-voltage-vector output time for the locus A of the previous magnetic flux vector, the locus A' is shorter than the previous one. Fig. ~~10 (3)~~10C is drawn by overlaying ~~(1) and (2) of Fig. 10~~ Figs. 10A and 10B on each other.

Replace the paragraph beginning at page 23, line 8 with:

In ~~Fig. 10 (1)~~ Figs. 10A and ~~(2)~~10B, magnetic flux vectors $\Phi 0$ and $\Phi 7$ are magnetic

flux vectors corresponding to the zero-voltage vectors V0 and V7. Since the zero-voltage vectors V0 and V7 do not have a magnitude, the magnetic flux vectors Φ0 and Φ7 each stay at one point even with time. A magnetic flux vector Φ1 is a magnetic flux vector corresponding to the voltage vector V1. The magnitude of the magnetic flux vector Φ1 is the product of the magnitude of the voltage vector V1 and its output time. A magnetic flux vector Φ2 is a magnetic flux vector corresponding to the voltage vector V2. The magnitude of the magnetic flux vector Φ2 is the product of the magnitude of the voltage vector V2 and its output time. As with the voltage vectors V1 and V2, the magnetic flux vectors Φ1 and Φ2 have a phase difference of $\pi/3$ radian.

Replace the paragraph beginning at page 24, line 6 with:

That is, when the output times of the zero-voltage vectors V0 and V7 are increased so that the relative ratio between the output times of the voltage vectors V1 and V2 is unchanged, the locus A of the magnetic flux before adjustment (Fig. ~~10 (1))~~ 10A)) is changed to the locus A' after adjustment (Fig. ~~10 (2))~~10B)). However, as shown in Fig. ~~5 (3)~~10C, a triangle formed by connecting a start point and an end point of the locus A' together in the PWM control cycle T is similar to a triangle formed by connecting a start point and an end point of the locus A together. Therefore, in a state where the cycle T is sufficiently short and the arc can be taken as a straight line, the end point of the locus A' is present on the arc, as is the case of the locus A. Therefore, if the voltage vectors are adjusted with the relative ratio between the output times of the voltage vectors V1 and V2 being unchanged, the locus A' of the magnetic flux after adjustment can also be made to smoothly go along the arc.

Replace the paragraph beginning at page 25, line 8 with:

Next, with reference to Figs. ~~12 and~~ 12A to 13, description is made to an effect of suppressing a surge voltage by keeping the output time of the zero-voltage vector at a time equal to or larger than the minimum zero-voltage-vector output time Tz. ~~Fig. 12 is a drawing~~ Figs. 12A to 12D are drawings for explaining a relation between the progression of the voltage vectors and line-to-line voltages. Fig. 13 is a drawing that depicts line-to-line voltage patterns extracted in view of a pulse polarity, an output time of the zero-voltage vectors, and output times of voltage vectors other than the zero-voltage vectors.

Replace the paragraph beginning at page 26, line 4 with:

~~Fig. 12 is a diagram~~ Figs. 12A to 12D are drawings depicting the four types of progression of the voltage vectors shown in ~~(1) to (4)~~ above with line-to-line voltage waveforms. It is understood from ~~Fig. 12~~ Figs. 12A to 12D that a pulse of a line-to-line voltage may be changed around the zero-voltage vector ~~in~~ with the same polarity or may be changed around the zero-voltage vector ~~in~~ with different polarities. Fig. 13 is a drawing that depicts line-to-line voltage patterns extracted from ~~this Fig. 12~~ Figs. 12A to 12D in view of a pulse polarity, ~~an~~ output time of the zero-voltage vectors, and output times of voltage vectors other than the zero-voltage vectors. ~~In~~ As shown in Fig. 13, for combinations of long and short output times of the zero-voltage vectors and long and short output times of the voltage vectors other than the zero-voltage vectors, a line-to-line voltage pattern 1 may be produced in which the voltage ~~is changed~~ changes around the zero-voltage vector ~~in~~ with the same polarity, and a line-to-line voltage pattern 2 may be produced in which the voltage ~~is changed~~ changes around the zero-voltage vector ~~in~~ with different polarities. All line-to-line voltage changes shown in ~~Fig. 12~~ Figs. 12A to 12D are classified into the eight types shown in Fig. 13.

Replace the paragraph beginning at page 26, line 20 with:

~~Fig. 14 depicts~~ Figs. 14A to 14H depict the magnitude of each surge voltage occurring in the changes in line-to-line voltage shown in Fig. 13. As evident from ~~Fig. 14~~ Figs. 14A to 14H, ~~as~~ for ~~(1-3), (1-4), (2-3)~~Figs. 14C, 14D, 14G, and ~~(2-4)~~ 14H where the zero-voltage-vector output time is long, no surge voltage exceeding twice the direct-current bus voltage Vdc occurs. On the other hand, ~~as~~ for ~~(1-1), (1-2), (2-1)~~ Figs. 14A, 14B, 14E, and ~~(2-2)~~ 14F where the zero-voltage-vector output time is short, a surge voltage exceeding twice the direct-current bus voltage Vdc occurs. It is therefore understood that appropriate selection of the output time of the zero-voltage vectors can suppress the occurrence of a surge voltage exceeding twice the direct-current bus voltage Vdc.

Delete paragraph beginning at page 28, line 1:

~~Second Embodiment~~

Replace the paragraph beginning at page 29, line 24 with:

Next, with reference to Figs. 13~~ and 14~~ to 14H, ~~an effect of~~ suppressing a surge voltage by making the output time of the zero-voltage vectors zero is described. As for (1-1) and (1-2) in~~ Figs.~~ Fig. 13 and~~ 14~~ Figs. 14A and 14B, outputting a short zero-voltage vector itself is a cause of a surge voltage exceeding twice the direct-current bus voltage Vdc. In~~ (1-1)~~ Figs. 14A and ~~(1-2) of Fig. 14~~ 14B, if no zero-voltage vector is present, one short pulse and one long pulse are present, which is equivalent to a waveform in a half cycle of~~ (1-3)~~ Figs. 14C and~~ (1-4)~~ 14D.

Delete the paragraph beginning at page 31, line 11:

~~Third Embodiment~~

Delete the paragraph beginning at page 36, line 4:

~~Fourth Embodiment~~

Delete the paragraph beginning at page 39, line 6:

~~Fifth Embodiment~~

Replace the paragraph beginning at page 42, line 5 with:

Furthermore, when the vector last output at the previous time is not a zero vector~~ (step 52: No)~~ (step ST52: No), the procedure branches to a sequence in which the procedure starts with a non-zero-voltage vector. At step ST56, when the total zero-voltage-vector output time t0+t7 is longer than 1/2 of the minimum zero-voltage-vector output time Tz (step ST56: Yes), the output time of the zero-voltage vector V0~~ to be~~ as the first output in the cycle is made zero (t0'=0), and the output time of the zero-voltage vector V7~~ to be~~ as the last output in the cycle is adjusted to the total zero-voltage-vector output time t0+t7 (t7'=t0+t7). Furthermore, as for the output times of the non-zero-voltage vectors V1 and V2, the output times t1 and t2 at this time are directly taken as adjusted output times t1' and t2' (step ST57).

Delete the paragraph beginning at page 44, line 4:

~~Sixth Embodiment~~

Replace the paragraph beginning at page 44, line 5 with:

Fig. 21 is a flowchart for explaining the operation of a voltage-vector adjusting unit included in a power-converter control apparatus according to a sixth embodiment of the present invention. In the power-converter control apparatus according to the sixth embodiment, in the structure shown in the fifth embodiment (Fig. 19), some functions are added to the voltage-vector adjusting unit 31. That is, the voltage-vector adjusting unit 31 according to the sixth embodiment performs an adjusting operation by using an output time of a zero-voltage vector last output in the previous PWM control cycle to determine an output time of a zero-voltage vector to be first output in the present PWM control cycle. With reference to Fig. ~~20~~ 21, the operation of the voltage-vector adjusting unit 31 according to the sixth embodiment is described below. In Fig. 21, procedures identical to those shown in Fig. 20 are provided with the same reference numerals. Here, description is made mainly to portions specific to the sixth embodiment.

Delete the paragraph beginning at page 47, line 10:

~~Seventh Embodiment~~

Replace the paragraph beginning at page 48, line 5 with:

Next, with reference to Figs. 22 through ~~24~~ 24C, the operation of the voltage-vector adjusting unit 41 in the power-converter control apparatus according to the seventh embodiment is described. Fig. 23 is a flowchart for explaining the operation of the voltage-vector adjusting unit 41 shown in Fig. 22. ~~Fig. 24 is a drawing~~ Figs. 24A to 24C are drawings for explaining an error-calculating operation ~~to be~~ performed by the voltage-vector adjusting unit shown in Fig. 22.

Replace the paragraph beginning at page 49, line 9 with:

Next, with reference to ~~Fig. 24~~ Figs. 24A to 24C, a method of calculating the error Err is described. In Fig. ~~24 (1)~~24A, loci A and B of magnetic flux vectors for two PWM control cycles before voltage vector adjustment are shown. The locus A is in the previous cycle, while the locus B is the current cycle. In Fig. ~~24 (2)~~24B, loci A' and B' of magnetic flux vectors after voltage vector adjustment are shown. As a result of ensuring the minimum zero-voltage-vector output time with the locus A of the magnetic flux vectors at the previous time, it becomes the locus A' with its length being shortened. Fig. ~~24 (3)~~24C is drawn by overlaying ~~(1)~~ Fig. 24A ~~and (2) of Fig. 24 each other~~ on Fig. 24B.

Replace the paragraph beginning at page 49, line 9 with:

Here, consider the case where the end point of the locus of the magnetic flux vectors before adjustment is made to agree with that after adjustment by drawing a locus as shown in the locus B' in the present PWM control cycle. As has been described in the first embodiment ~~(Fig. 10)~~, (Figs. 10A to 10C), when the voltage vectors are adjusted according to equation 3 so that the relative ratio of the output times of the voltage vectors other than the zero-voltage vectors is unchanged, a triangle of the locus A is similar to a triangle of the locus A'. Similarly, a triangle of the locus B is similar to a triangle of the locus B'.

Delete the paragraph beginning at page 51, line 7:

~~Eighth Embodiment~~

Replace the paragraph beginning at page 51, line 21 with:

That is, taking note of Fig. ~~12(1)~~12A, eliminating the zero-voltage vector V7 does not pose the line-to-line voltages Vvw and Vwu. However, as for the line-to-line voltage Vuv, two pulses of the voltage vector V1 are present over the voltage vector V2. This corresponds to the case of ~~(1-2) of Fig. 14~~ Fig. 14B, with the voltage vector V2 being replaced by the zero-voltage vector. That is, when the output time of the zero-voltage vector is adjusted to zero, depending on the non-zero-voltage-vector output time, a surge voltage may occur. In such a case, in the ~~eight~~ eighth embodiment, the concept of ensuring the minimum zero-voltage-vector output time is applied. Hereinafter, a description is ~~made~~ implied according to

Fig. 25.

Replace the paragraph beginning at page 52, line 21 with:

As a result, when the adjusted output time t2' of the voltage vector V2 is shorter than 1/2 of the minimum zero-voltage-vector output time Tz ~~(step S83: Yes)~~ (step ST83: Yes), the adjusted output time t2' is readjusted to t2'=Tz/2. At this time, the adjusted output time t1' of the voltage vector V1 is readjusted to t1'=T-Tz/2 (step ST84).

Delete the paragraph beginning at page 53, line 22:

~~Ninth Embodiment~~

Replace the paragraph beginning at page 53, line 23 with:

Fig. 26 is a flowchart for explaining the operation of a voltage-vector adjusting unit included in a power-converter control apparatus according to a ninth embodiment of the present invention. In Fig. ~~25~~ 26, procedures identical or equivalent to those shown in Fig. 20 (the fifth embodiment) are provided with the same reference numerals. Here, description is made mainly to portions specific to the ninth embodiment.

Replace the paragraph beginning at page 54, line 10 with:

That is, when the pattern of the occurrence of a surge voltage is ~~(2-1) or (2-2) of Fig. 14~~ as in Figs. 14E and Fig. 14F, the surge voltage of the motor-end line-to-line voltage cannot be suppressed, even ~~with~~ by elimination of the zero-voltage vector. Therefore, taking not ~~to (3)~~ of Figs. 12C and ~~(4) of Fig. 12~~ 12D, in ~~(4) of~~ Fig. 12D, the phenomena in ~~(2-1)~~ Figs. 14E and ~~(2-2) of Fig. 14 occurs~~ 14F occur. It is evident, however, that such a phenomenon does not occur in ~~(3) of~~ Fig. 12C. The progression of the voltage vectors when the phase θ makes a transition from a range of $0 \leq \theta < \pi/3$ to a range of $\pi/3 \leq \theta < 2\pi/3$ is shown below again.

(3) V0→V1→V2→V7→V2→V3→V0

(4) V7→V2→V1→V0→V3→V2→V7

Here, the progression becomes as follows when the zero-voltage vectors are eliminated.

(3)' V0→V1→V2→(V7)→ V2→V3→V0

(4)' V7→V2→V1→(V0)→V3→V2→V7

From comparison with (3)' and (4)', it is evident that the phenomena in ~~(2-1)~~ Figs. 14E and ~~(2-2) of Fig. 14~~ 14F are eliminated when the voltage vectors before and after elimination of the zero-voltage vectors are made identical to each other, thereby suppressing a surge voltage.

Replace the paragraph beginning at page 56, line 5 with:

As such, according to the ninth embodiment, the cases of ~~(2-1)~~ Figs. 14E and ~~(2-2) of Fig. 14~~ 14F occurring when the output times of the zero-voltage vectors are adjusted to zero can be avoided. Therefore, a surge voltage exceeding twice the direct-current bus voltage Vdc can be reliably suppressed. Also, an effect of such suppression of a surge voltage can be obtained over all ~~phase~~ phases only by adjusting the voltage-vector output times, which are parameters that are common to three phases.